Record Efficiency and Gain at 2.1GHz of High Power RF Transistors for Cellular and 3G Base Stations

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Abstract

Improved RF performance of Motorola's next generation HV6 high power RF-LDMOS transistor is demonstrated. In the 2.1GHz band with a two-carrier WCDMA signal, a 29% drain efficiency is achieved at -37dBc IM3 and 20W of output power, along with a high power gain of over 16.5dB. To our knowledge this is the highest combination of efficiency and linearity ever reported on a high power part of any technology or material system in that frequency band. A PAE of 62% at 100W (P_{3dB}) is also achieved.

Introduction

RF-LDMOS power transistors have acted as the work horse technology in broadcast and cellular base stations for many years. They have proven to be very reliable, consistent and cost effective. 3G systems require high power transistors with high efficiency and linearity. The high power RF performance of RF-LDMOS has not been matched by transistors of any technology or material in production. Power amplifier and base station manufacturers are pressured more than ever to reduce their hardware and maintenance costs. The power amplifier line-up with the output stage is one of the biggest single cost items. Costs for the transistors, manufacturing and maintenance are directly related to the part's ease-of-use, consistency, thermal performance, efficiency, gain and reliability. LDMOS has proven to be the technology of choice to best meet all those demands. In this paper the advancements of the next generation LDMOS are presented.

RF-LDMOS Device Structure

Fig. 1 shows a schematic cross section of the sixth generation (HV6) RF-LDMOS device. It includes a p+ sinker to connect the back side source contact through a p+ substrate to the top side intrinsic source. A low concentration drift region between the gate and the highly doped drain contact is designed to support high breakdown voltages along with a low doped epi. The aluminum stacked drain metal is designed to meet electromigration specifications for high reliability. A metal-2 gate bus running parallel to the gate periodically makes connections to the gate WSi/Poly stack to reduce its resistance. A grounded thin WSi shield between the gate and the drain metal acts to reduce the feedback capacitance Cgd.

DC Characteristics

Optimization of the drift region resulted in a BVdss of 72V with a very low Rdson of about 14.5 Ωmm; the Rdson of

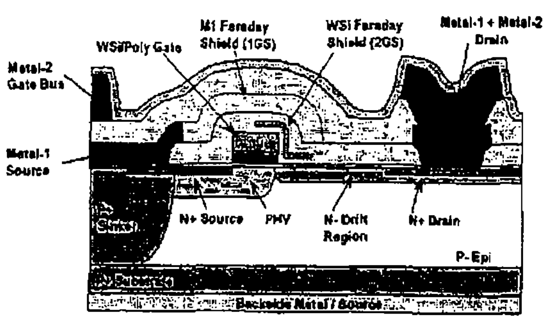

Fig. 1. Schematic x-section of a high voltage RF-LDMOS.

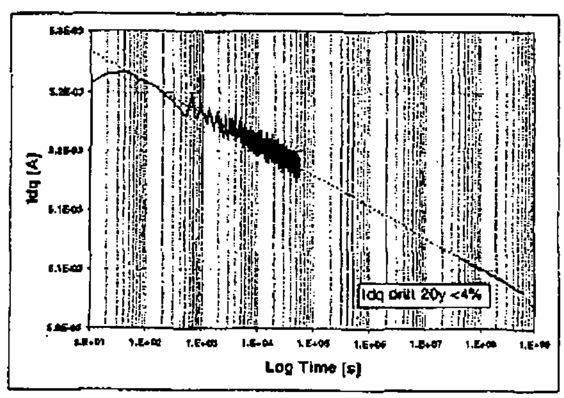

Fig. 2. Measured Idq drift (16h) with extrapolation to 20y.

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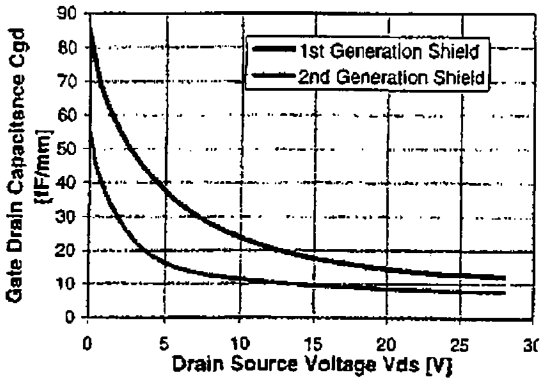

Fig. 3. Cgd for 1st and 2nd generation Faraday shield.

this demo device is ~25% lower than the previous HV5 platform. The drift region optimizations did not sacrifice the state-of-the-art HCI reliability measured in a 16h stress test at room temperature. Fig. 2 indicates a typical Idq drift of less than 4% extrapolated to 20 years.

Small Signal Performance

Significant improvements were made by incorporation of a 2nd generation Faraday shield (2GS, shown in Fig. 1) to substantially reduce the feedback capacitance of the device. Fig. 3 shows the Cgd improvement compared to an already low value using a 1st generation Faraday shield (indicated as dotted lines in Fig. 1). Besides increasing gain low feedback capacitance improves ruggedness and ease-of-use of the device. Both attributes are important for scaling the device to the large peripheries needed for high power parts. To further

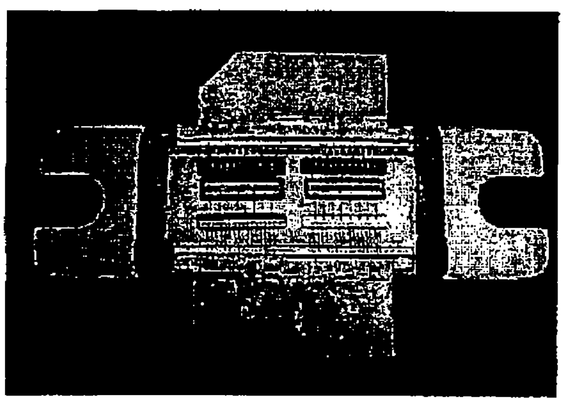

Fig. 4. 90W single-ended device with two die, input and output matching.

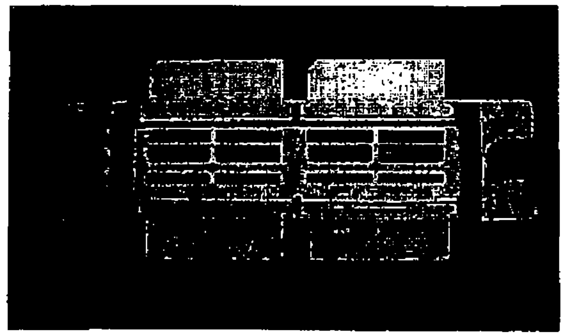

Fig. 5. 170W (P_{1dB}) push-pull device with four 60mm die, input and output matching.

increase the high frequency gain of the device, the gate length and oxide thickness were reduced to 500nm and 300A, respectively, resulting in an f_T and f_{max} of 8 GHz and 12 GHz, respectively, along with a small signal gain of 25.5 dB.

High Power RF Performance

High power device performance is demonstrated on two devices: a single-ended part using two RF-LDMOS die (Fig. 4) and a push-pull part with four die (Fig. 5). Each die has a gate periphery of 60mm. Both devices are input- and

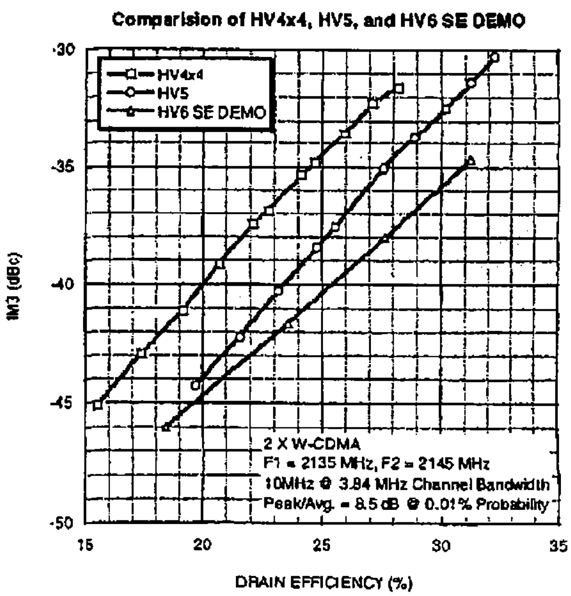

Fig. 6. IM3 versus drain efficiency under a 2 carrier WCDMA 2.1GHz signal for single ended HV4x4, HV5 and new demo part.

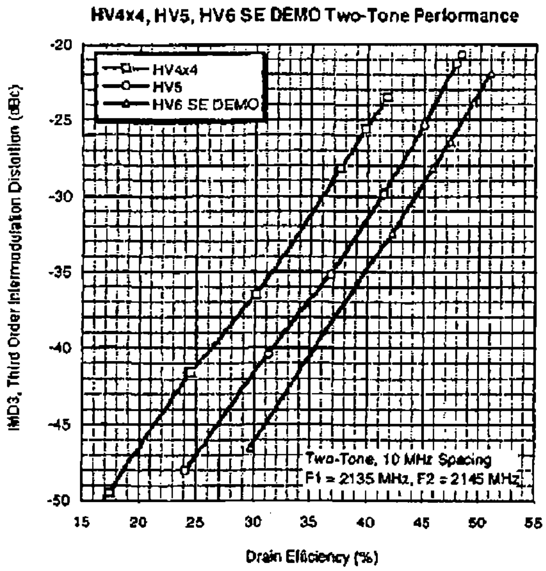

Fig. 7. IM3 versus drain efficiency under a 2 tone 2.1GHz signal for single ended HV4x4, HV5 and new demo part.

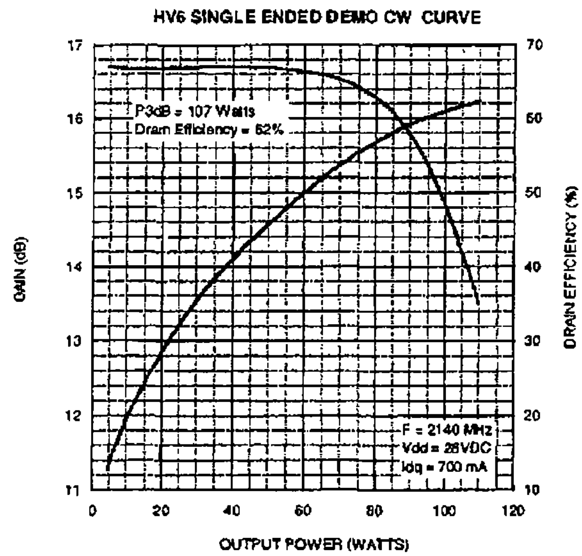

Fig. 8. Power gain and output power of the new single ended demo part with a 2.1GHz CW single tone.

output-matched to increase the impedance levels for improved matching across the frequency band and ease-of-use. The devices were tuned in a fixture using a 2-carrier WCDMA signal at 2.14GHz. The linearity is measured as the ratio of the power in the upper and lower 3rd intermodulation product (IM3) to the power in the carrier signal. The tuning of the device includes performance trade-offs to obtain necessary gain flatness across the band and a maximum input return loss (IRL) of −10dB. The performance is optimized at an IM3 of −37dBc. The HV6 device WCDMA linearity-efficiency performance compared to the two latest RF-LDMOS generations (HV4X4 and HV5) is shown in Fig. 6 [1]. The graph shows IM3 versus efficiency for a single ended device as the input power is ramped up. An efficiency improvement for the HV6 part at a linearity level of −37dBc IM3 of about 3% over HV5 is achieved. Similar improvements are obtained under two-tone evaluation at 2.1GHz as shown in Fig. 7. In this case the part is measured with single tones rather than two frequency bands. A 3% efficiency improvement was obtained for the entire high power part of the curve.

The CW performance at 2.14GHz is depicted in Fig. 8. The gain of the HV6 demo device exceeds 16.5dB. It reaches an output power of about 90W at 1dB of gain compression along with a drain efficiency of about 59%. An efficiency of about 62% is reached for P_{3dB} with an output power of 107W. This translates into a power density of 890mW/mm.

The performance for the corresponding push-pull part is

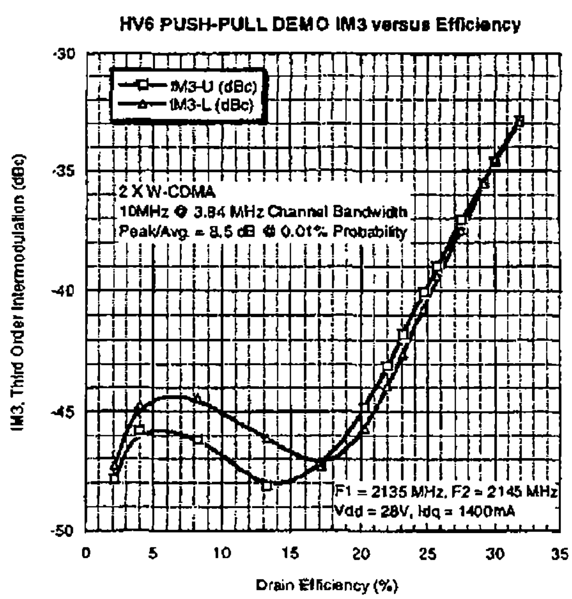

Fig. 9. IM3 versus drain efficiency under a 2 carrier WCDMA 2.1GHz signal for the new push pull demo part.

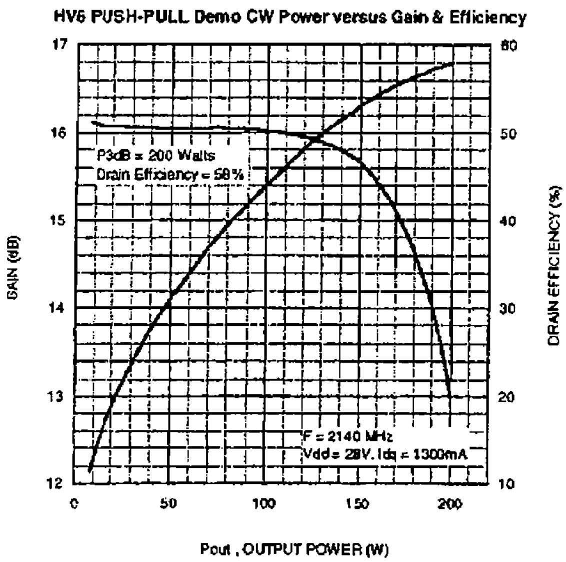

Fig. 10. Power gain and output power of the new push pull demo part with a 2.1GHz CW single tone.

shown in Fig. 9 and Fig. 10. In this case the same die as in the single-ended version were used except now in a 2x2 configuration as shown in Fig. 5. Fig 9 shows the upper and lower IM3 versus efficiency as the power is ramped up. In back-off the ΔIM3 is less than 2dB. For the high power part of the curve the ΔIM3 is reduced to less than 1dB. The efficiency at the -37dBc point is nearly 28% and the power gain is still about 16dB. This translates into an efficiency of about 55% and 58% at 170W (P_{1dB}) and 200W (P_{3dB}), respectively for CW operation. This is a power density of 830mW/mm. The reduction in efficiency and gain for the push-pull version compared to the single ended part is consistent with an expected 0.3dB of combining losses.

Impact on a Multistage Amplifier Line-up

The demonstrated efficiency increases mainly improve the system efficiency of a base station through improvements in the output stage of the power amplifier. However, the high gain of the transistor offers significant savings and improvements. For a drain efficiency of 30%, PAE is increased from 28.5% to 29.3% for a gain increase from 13 to 16dB. Moreover, higher gain reduces the power requirement in driver stages which enables replacement of multi-stage driver line-ups with a much lower power high gain block like a module with an additional increase is overall PAE for the full line up. The total cost savings are considerable. An example of a possible line-up change is depicted in Fig. 11.

Part	[illegible]	[illegible]	[illegible]	Total	[illegible]	[illegible]	Total
Typ Gain	[illegible]	[illegible]	11.7dB	[illegible]	[illegible]	17dB	[illegible]
Pout	[illegible]	4.5W	[illegible]		[illegible]	[illegible]	
Efficiency	3%	16%	22%	[illegible]	[illegible]	[illegible]	[illegible]
Current	[illegible]	1A	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Fig. 11. Comparison a conventional 3-stage line-up with low gain output stage compared to a possible line up with a high gain output stage.

Conclusions

In the 2.1GHz band with a two-carrier WCDMA signal, a 29% drain efficiency is achieved at -37dBc IM3 and 20W of output power, along with a high power gain of over 16.5dB. To our knowledge this is the highest combination of efficiency and linearity ever reported on a high power part of any technology or material system in that frequency band. A PAE of 62% at P_{3dB} with 107W is also achieved, which represents a power density of 890mW/mm. The combination of efficiency and gain increase has a very substantial impact at the system level by improving performance reducing power requirements for drivers and enabling simpler, lower cost line-up configurations.

Acknowledgment

The authors would like to thank Leonard Pelletier for input and discussions on line-up configurations as well as Richard Pearl for HCI stress tests.

References

[1] Chris Dragon, et al., "200W Push-Pull & 110W Single-Ended High Performance RF-LDMOS Transistors for WCDMA Basestation Applications," *IEEE MTT-S Int. Microwave Symp. Dig.*, Philadephia, Pennsylvania, June 8-13, 2003, TU3B-1, pp. 69-72.